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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,576	07/28/2003	John LeRoy Parker JR.	8245.057	5022
30589	7590	04/04/2007	EXAMINER	
DUNLAP, CODDING & ROGERS P.C. PO BOX 16370 OKLAHOMA CITY, OK 73113			LAM, CATHY FONG FONG	
			ART UNIT	PAPER NUMBER
			1775	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,576	PARKER ET AL.	
	Examiner	Art Unit	
	Cathy Lam	1775	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 January 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 46-62 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 46-62 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 17 January 2007 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>1-26-2007</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____.

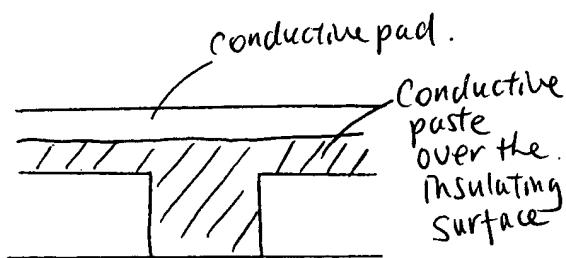
In view of the amendment and remarks filed on January 17, 2007, the 112 rejections have been withdrawn. The pending claims however continue to be unpatentable as following:

Drawings

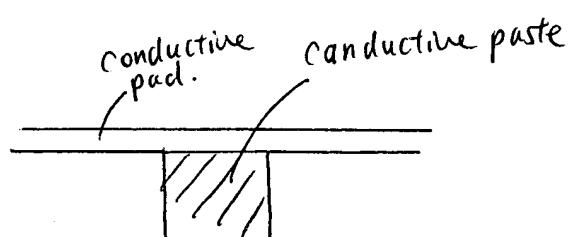
1. The drawings were received on January 17, 2007. These drawings containing numeral that are not described in the specification. Numerals 12a, 14a, 16a, 18a....etc. are not defined in the specification. Applicant is required to be consistently throughout when choosing the numerals to depict the figures.

Claim Rejections - 35 USC § 112

2. Claim 46 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended portion has completely changed the scope of the original invention. Applicant is kindly asked to point out to the examiner where this limitation was derived from.



Amended claim 46



previous claim 46.

Claim Rejections - 35 USC § 102/103

1. Claims 46-62 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Mizumoto et al (US 5662987).

Mizumoto teaches a multilayer printed wiring board comprised of two or more stacked layers of with conductive blind via holes (Figs 12, 13 and 19).

Each layer comprised of an insulating layer with a via hole formed in the thickness direction of the insulating layer. A first conductive layer (540) formed from the top surface of the insulating layer and plating the via hole surface and closed the bottom side (here refer to 2nd side), the examiner is taking the position that this is a blind via hole (Fig. 19).

Electrically conductive material (530) is filled into the blind via, and it is filled over the surface of the insulating layer and flushed (or leveled) with the first conductive layer (540) (Fig. 18). Then, a second conductive layer (560) is plated over the first conductive layer (540) and the electrically conductive material (530) (col 5 L 55-58 & Fig. 19).

The electrically conductive material is a conductive paste comprised of copper filler and a resin material (col 4 L 21-25).

Mizumoto teaches the concept of the present invention but is silent about the thickness of the 1st conductive layer.

The examiner is taking the position that one skill in the art would choose a workable thickness for the invention because it is just a matter of design choice.

2. Claims 46-62 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ishikawa et al (US 5243142).

Ishikawa discloses a printed wiring board comprised of an insulating substrate (1), a via hole (3), a first plating layer (4), a second plating layer (6) and a non-electroconductive resin paste (5).

The via hole if formed in the insulating substrate and is plated with the first plating layer (4). The first plating layer (4) is a copper layer that plates over the both surfaces and the via hole surface of the insulating substrate (col 2 L 30-34).

A non-electroconductive resin paste (5) that containing a metal powder is used to filled into the plated via hole. Then a second plating layer (6) which is also a copper layer is plated over both surfaces of the insulating substrate and completely covers the first plating layer (4) and the resin paste (5) (col 3 L 52-55). The first and second plating layers (4 & 6) would be formed into a circuit pattern (col 5 L 49-53, Fig. 4).

The prior art teaches the present invention except for the resin paste in the via hole is non-electroconductive. The prior art also does not teach the thickness of the Cu plating layer being < 0.2 mil.

Ishikawa teaches the non-electroconductive resin paste that containing metal powder, the amount of metal powder is a controlled amount, so that it would not to increase electroconductivity (col 2 L 60-65).

In view of Ishikawa's teaching, one skill in the art would choose an electroconductivity for the via hole resin paste by adjusting the amount of metal powder because it is just a matter of design choice. Furthermore, one skill in the art would

certainly choose a desirable thickness for the conductive pads or wiring patterns because it is only a matter of design choice.

Ishikawa's second plating layer (6) is plated over the first plating layer and seals off both ends of the via hole resin paste; according to the newly added claims, the examiner is taking the position that Ishikawa's structure is both a buried via and a through hole blind via.

Response to Arguments

3. Applicant's arguments filed January 17, 2007 have been fully considered but they are not persuasive. Applicant traverses the art rejection and raises the following issues:

- A. The prior art does not teach a cured mass of a flowable conductive material extending over the first surface and filling said blind via.
- B. Mizumoto does not teach or suggest extending over the first surface, but rather only over the uppermost portion of the plated layers.

In respond to the above issues:

- A. This newly added limitation is not supported by the original specification, applicant has changed the scope of the present invention from one structure to another structure.
- B. Mizumoto shows that the plating layer (390) is over the (1st) plated layer (330) and the conductive paste (340) underneath, however having the (1st) plated layer (330) over the entire insulating layer surface and having the plating layer over the (1st) plated layer (330) would be an obvious variation. Besides applicant's invention is intended to have the plating layers to be formed into conductive pads and/or patterns. Mizumoto's

structure perhaps can be view as a final product of the present invention, because the plating layers are formed into a conductive pad or a conductive pattern.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cathy Lam whose telephone number is (571) 272-1538. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on (571) 272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Cathy Lam
Primary Examiner
Art Unit 1775

cfl
July 01, 2006